The attention of the Examiner is directed to the filing of an Amendment under 37 CFR 1.607 in Serial No. 08/504,225, the '225 application being the parent of the present Rule 60 divisional application. In particular, the purpose of the foregoing Amendment under 37 CFR 1.607 is to initiate an interference with respect to the device claims of the above-mentioned '366 patent.

Moreover, an Amendment under 37 CFR 1.607 has also been filed in application Serial No. 08/223,823 to also initiate an interference with the foregoing '366 patent. In fact, the claims added to the '225 application are exactly the same as those added to the '823 application. In this regard the issue fee was paid in the '823 application on April 7, 1997, and thus a Petition under 37 CFR 1.313(b)(4) has also been filed to withdraw the '823 application from issue.

Furthermore, upon grant of the foregoing Rule 313(b)(4) Petition and declarations of interferences in the '225 and '823 applications, it has been requested that the foregoing interferences be consolidated into a single interference in view of the fact that the claims added to the '225 and '823 applications are exactly the same.

New claims 23-32 in this Rule 60 divisional application are substantially copied from U.S. Patent No. 5,561,075 to Nakazawa (hereinafter Nakazawa '075 or the '075 patent), a copy of which is submitted herewith. Claims 23-24 and 29-32 are exactly the same as claims 1-2, and 9-12 of the '075 patent and claims 25-28 are generally related to claims 3 and 6-8 of the '075 patent. In accordance with 37 CFR §1.607(a)(5), copied claims 23-32 may be applied to applicant's disclosure as shown in the claims analysis attached thereto as Exhibit A.

In accordance with 37 CFR §1.607(a)(2), applicant presents the following proposed count 1, wherein claim 1 of the '075 patent and claim 23 submitted herewith each correspond exactly to count 1:

1. A method of manufacturing an active matrix panel in which data signals are supplied to liquid crystal layers through a plurality of thin film transistors arranged in a matrix of pixels, gate lines and data lines being coupled to each thin film transistor, said method comprising the steps of:

forming a semiconductor layer on a substrate;

forming a gate insulating film on said semiconductor layer;

forming a gate electrode above said gate insulating film and a gate line in electrical contact with said gate electrode;

forming a source region and a drain region in said semiconductor layer by adding impurities thereto as donors or acceptors using said gate electrode as a self alignment mask;

simultaneously forming an overlying gate insulator on a top and sidewalls of said gate electrode and said gate line by anodic oxidation of said gate electrode and said gate line to reduce the dimensions of said gate electrode and said gate line and simultaneously form a lateral offset, ΔL, from said source region and said drain region to the sidewalls of said gate electrode; and

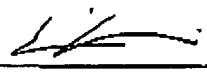
forming a data line in electrical contact with said source region and crossing over said gate line at a cross-over location, wherein said overlying gate insulator is located between said data line and said gate line at said cross-over location to insulate said data line from said gate line.

With respect to the foregoing, the attention of the Examiner is directed to the fact that, during the prosecution of application Serial No. 07/880,120 (a predecessor application upon which the '075 patent is based), the party Nakazawa filed a verified English translation of one of their Japanese priority applications on July 13, 1994 in order to avoid a rejection under 35 U.S.C. § 102 based on U.S. Patent Number 5,289,030, which patent

issued on a predecessor application of the subject application. In particular, the party Nakazawa attempted to obtain a Japanese filing date earlier than the effective U.S. filing date of the subject application. However, as demonstrated herein and below, the present applicant is entitled to an earlier Japanese filing date than the earliest Japanese filing date of the party Nakazawa with respect to at least claims 23, 25-29, and 31-32.

Verified English translations of the Japanese priority applications (Nos. 3-65418 filed March 6, 1991 and 3-135569 filed May 11, 1991) for the present application are submitted herewith. Newly presented claims 23-32 can be read on these priority applications as shown in Exhibit B. As can be seen, applicant is entitled to the March 6, 1991 priority date for at least claims 23, 25-29 and 31-32. Since applicant's March 6, 1991 priority date is earlier than the May 8, 1991 priority date of the '366 patent, applicant respectfully requests that it be designated senior priority in a declaration of the interference.

Respectfully submitted,



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